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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,347	01/23/2004	Yoshikazu Takahashi	32305-200192	4869

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,347	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-49,52-55 and 58-62* is/are rejected.

7)☒ Claim(s) *50,51,56,57,63 and 64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-23-04 & 3-2-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the preliminary amendment filed January 23, 2004.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 46-49, 52-55 and 58-62 are rejected under 35 U.S.C. 102(e) as being anticipated by Murayama (5,736,780).

In regard to claim 46, Murayama teaches a semiconductor device comprising: a semiconductor chip 12 having a main surface, a back surface and a plurality of side surfaces; a plurality of electrodes arranged in a plurality of lines on the main surface of the semiconductor chip 12; a base resin film 34 formed on the main surface of the

semiconductor chip 12, the base resin film 34 having a first surface facing the main surface of the semiconductor chip 12, a second surface opposite to the first surface and a through hole provided thereof; a plurality of conductive patterns 30 formed on the first surface of the base resin film 34, the conductive patterns 30 extending near the through hole; and an insulating film formed 44 on the first surface of the base resin film 34 and the conductive patterns 30, the insulating film 44 having a plurality of electrode holes for exposing a part of the conductive patterns 30 through the through holes (Figures 6 and 8, columns 7-8, lines 13-46 and 10-23, respectively).

In regard to claim 52, Murayama teaches a semiconductor device comprising: a semiconductor chip 12 having a main surface, a back surface and a plurality of side surfaces; a plurality of electrodes arranged in a plurality of lines on the main surface of the semiconductor chip 12; a base resin film formed on the main surface of the semiconductor chip, the base resin film having a first surface said semiconductor chip, a second surface opposite to the first surface and a through hole provided thereof; a plurality of conductive patterns 30 formed on the second surface opposite the first surface and a through hole provided thereof; a plurality of conductive patterns 30 formed on the second surface of the base resin film 34, the conductive patterns 30 extending near the through hole; an insulating film 44 formed on the second surface of the base resin film 34 and conductive pattern 30, the insulating film 44 having a plurality of electrodes holes for exposing a part of the conductive patterns 30; and a plurality inner leads 30c connecting the electrodes with the conductive patterns 30 through the through holes (Figures 6 and 8, columns 7-8, lines 13-46 and 10-23, respectively).

In regard to claim 58, Murayama teaches a semiconductor device comprising: a semiconductor chip 12 having a main surface, a back surface and a plurality of side surfaces; a plurality of electrodes arranged in a plurality of lines on the main surface of the semiconductor chips 12 the base resin 34 film having a first surface facing said semiconductor chip 12 and a second surface opposite the first surface; a plurality of electrode patterns 30 formed on the first surface of the base resin film 34; a first insulating film 44 formed on the first surface of the base resin film 34, the first insulating film 44 having a plurality of first electrode holes for exposing the electrode patterns 30; a plurality of conductive patterns 30c formed on the second surface of the base resin film 34, the conductive patterns 30c electrically connected to the electrode patterns 30; and a second insulating film 22 formed on the second surface of the base resin film 34 and the conductive patterns 30c, the insulating film having a plurality of second electrode holes for exposing a part of the conductive patterns 30c (Figures 6 and 8, columns 5 and 7-8, lines 9-16, 13-46 and 10-23, respectively).

In regard to claims 47, 53 and 59, Murayama teaches the main surface and side surface of the semiconductor chip covered by molding resin (Figures 6, column 7, lines 13-22).

In regard to claims 48, 54 and 60, Murayama teaches a plurality of solder balls 14 formed on the electrode holes (Figures 6 and 8, columns 7-8, lines 13-46 and 10-23, respectively).

In regard to claims 49, 55 and 61, Murayama teaches the base resin film 28 & 34 formed on the main surface, back surface and side surface of the semiconductor chip 12 (Figures 6 and 8, columns 7-8, lines 13-46 and 10-23, respectively).

In regard to claim 62, Murayama teaches the base resin film 28 & 34 substantially surrounding the semiconductor chip (Figures 6 and 8, columns 7-8, lines 13-46 and 10-23, respectively).

Allowable Subject Matter

Claims 50-51, 56-57 and 63-64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor device structures:

Behlen et al. (5,598,033) DiStefano et al. (5,801,441)

Kitano et al. (5,608,265) Paurus et al. (5,448,511).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-

1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
June 27, 2005

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